

**TEK07061** (Altium - 9 + Year)

Highlights

Objective

To be successful, with affirmative approach to handle my responsibilities with zeal and the full application of my knowledge that possess to work as a team and stand up to the expectation of the concern

EXPERIENCE SUMMARY

- Schematic Design, aware about the Polarized Components & Effective Utility of Heterogeneous part, Trouble shoots error and Net-list Extraction
- Schematic symbols are created as per the IEEE standards
- PCB footprints as per the IPC-7351B standards
- Footprint created as per Customer defined guidelines
- Designing of Single, Double & Multilayer PCBs
- Critical Components Placement with proper guideline standard
- Knowledge in DFA, DFM and DFT
- Take care about EMI and EMC
- Take care to maintain Signal Integrity
- Knowledge of Impedance Matching based on the Layer Stack-Up Structure
- Aware about Signal Parallelism
- Better Plan to run Critical Signals with separate & shielded Ground-Reference
- Maintain the Balanced Copper density in each individual layer
- Advanced knowledge of constraints set
- Expertise in usage of Blind & Buried vias
- Layout translation ? Schematic translation
- Knowledge of scripting and Documentation

HIGHLIGHTS AND SKILLS

- Used advanced HDI concept like blind and buried via.
- Worked with multiple BGA designs (0.5 mm,0.65 mm,0.8 mm)
- Work experience with high-speed interfaces like DDR3, DDR4, HDMI, PCIe, USB, Ethernet RJ45, LVDS,QSFP,OCULINK,CAPI,M2 and SATA
- Designed PCB layouts for high frequency operations designs.
- Gained good knowledge of Google, Intel, Analog Devices, and IBM symbol/PCB land pattern standards.
- Worked with PCB reverse engineering concepts.
- Must be able to work on many different projects at one time and be results oriented
- Expertise in Signal Grouping, Pin-Pair settings & Length Matching for DDR Memory Slot
- Experience in Gerber Analyze & Net-list compare and Analyze in CAM350

Skills

Primary Skills

- Altium
- CAM 350

Secondary Skills

- Allegro

Other Skills

PCB DESIGN TOOL

1. Cadence Allegro v.17.4
2. Altium Designer v.20.2.3
3. Pads Layout v.9.5

SCHEMATIC TOOL

1. OrCAD Capture CIS,
2. Concept HDL
3. Altium Designer v.20.2
4. Pads logic

GERBER ANALYZE TOOL

1. CAM 350, View mate , Altium CAMtastic

Symbol / Library Creation

1. OrCAD, Concept HDL / Allegro 17.4, Altium20.0/ Pads And Expedition

Projects

(NX0503_385A-SOC)

Description

This is the 385A-SoC System on Chip FPGA Accelerator Card

- 16 Layers with the size of 6.5"X3"
- Total number of Components 1002
- Altera Arria 10 SX F34 package
- Main Processor BGA with 1152pins
- 2 Banks 4G DDR4 SDRAM
- 8-Lane PCI-Express Gen 3

Challenges, Technologies used

- 1mmpitch BGA Fan-out and Trace Out all signals in 8 Layers
- Length matching the DDR4 in Daisy Chain topology routing method for Address lines
- Narrow edge routing path to avoid stub, Proper Shield to avoid noise
- DDR4 Interface Routings, PCIe Express Interface
- It has lot of powers and impedances are used (12v,5v,3.3v,3v,2.5v,1.8v,1.2v ,0.9v,0.6v and40ohms, 50 ohms, 90 ohms, 95 ohms, 100 ohms)

Role & Contribution

- Lane Grouping & Length Matching and Mechanical check as per DXF

Tools & Gerber Verification

- Altium Designer 17.1 & CAM350

BR02-1180-01

Description

- This is the memory and data transfer card
- 16 Layers with the size of 5.6”X4.4”
- Total Number of components 1447
- Main Processor BGA with 780pins
- DDR4 Module
- ETHERNET 1G PHY INTERFACES
- QSGMI ETHERNET PHY
- NOR FLASH
- ETHERNET QUAD MAGNETICS
- RMI HIGH-SPEED CONNECTOR
- RF BOARD Connectors
- FRONT PANEL CONNECTOR
- REAR CONNECTOR

Challenges, Technologies used

- High Density Board with Critical Placement Constraint
- Fine pitch component 0.65mm Used
- High speed signal routing and length tuned
- Power plane handling
- It has lot of powers and impedances are used (12v,5v,3.3v,2.5v,1.8v,1.2v,1.1v,1.0v and 50ohms, 75 ohms, 85 ohms,100 ohms)

Role & Contribution

- Creating Board Outline with Mechanical Spec, Placement
- Constraint setup and Fanout
- Length matching and report added
- Fabrication setup
- Gerber generation and Cam verification

Tools

- Cadence Allegro 17.2, OrCAD Capture CIS

(NT-520N-MX)

Description

This is the High performance compute node featuring 3Dstacked High Bandwidth Memory (HBM2) and choice of external memory DIMMs

- 16 Layers with the size of 10.5”X3.87”
- Total number of components 1723
- Main Processor Stratix 10 FPGA with 2597pins
- DDR4 DIMM
- MAX10 FPGA
- USB 2.0 Micro USB
- Flash Memory
- PCI edge fingers
- QSFP28 Connectors
- PCIE_OCULINK Connectors

- 25G_OCULINK Connectors

Challenges, Technologies used

- High Density Board with Critical Placement Constraint
- Fine pitch component 0.5mm and 0.65 mm used
- High speed signal routing and length tuned
- PMIC Power fanout and power plane handling
- It has lot of powers and impedances are used (VCC_CORE -0.9v and(125A),12v,3.3v,2.5v,1.8v,1.2v and 40ohms, 80 ohms, 85 ohms, 90 ohms, 100 ohms)

Role & Contribution

- Constraint setup and Fanout
- Length matching and report added
- Fabrication setup
- Gerber generation and Cam verification

Tools

- Altium Designer 17.1 & CAM350